AMENDMENTS TO THE CLAIMS

Please add or amend the claims to read as follows, and cancel without prejudice or disclaimer to resubmission in a divisional or continuation application claims indicated as cancelled:

1.-2. (Cancelled)

3. (Currently amended) ~~The method according to claim 2~~ A method for verification of a system design represented by a model that includes a plurality of variables, the method comprising:

arranging the variables in an Ordered Binary Decision Diagram (OBDD) according to an initial order of the variables, the OBDD comprising a number of nodes arranged in rows corresponding respectively to the plurality of the variables;

assigning to each processor, among a group of two or more computer processors, a respective variable among the plurality of the variables;

using each processor, reordering the rows of the OBDD by varying a position in the OBDD of one of the rows, which corresponds to the respective variable that is assigned to the processor, until at least one of the processors identifies a new order for the OBDD; and

using the new order of the OBDD, verifying a characteristic of the model against a specification,

wherein reordering the rows comprises,

using each processor, finding the new order such that the number of the nodes in the OBDD is reduced relative to the initial order; and

~~, wherein reordering the rows comprises~~ receiving first and second new orders, respectively, from first and second processors among the two or more computer processors, and selecting the new order from among the first and second new orders so as to minimize the number of the nodes in the OBDD.

4. (Currently amended) The method according to claim [[1]] 3, wherein reordering the rows comprises operating simultaneously with at least two of the processors on a common set of the rows.

5. (Original) The method according to claim 4, wherein operating simultaneously comprises operating on substantially all the rows of the OBDD using all of the at least two of the processors.

6.-8. (Cancelled)

9. (Currently amended) The method according to claim [[7,]] 3, and comprising replacing the initial order with the new order, and repeating the steps of assigning the respective variable and reordering the rows based on the new order until a predefined reordering criterion is satisfied,

wherein the two or more computer processors comprise first and second processors, and wherein reordering the rows comprises receiving the new order from the first processor, and wherein replacing the initial order comprises communicating the new order to the second processor for use in repeating the step of reordering the rows.

10. (Original) The method according to claim 9, wherein reordering the rows comprises receiving first and second new orders, respectively, from the first and second processors, and selecting the first new order according to a predefined selection criterion.

11. (Currently amended) The method according to claim [[7,]] 3, and comprising replacing the initial order with the new order, and repeating the steps of assigning the respective variable and reordering the rows based on the new order until a predefined reordering criterion is satisfied,

wherein verifying the characteristic comprises operating on the OBDD using the group of computer processors while saving data regarding the OBDD in a memory until a predetermined amount of space in the memory has been consumed, and wherein

repeating the steps of assigning the respective variable and reordering the rows comprises repeating the steps after operating on the OBDD to verify the characteristic so as to reduce the amount of space occupied by the OBDD in the memory.

12.-27. (Cancelled)

28. (Currently amended) ~~The product according to claim 27,~~ A computer software product for verification of a system design represented by a model that includes a plurality of variables, the product comprising a computer-readable medium in which program instructions are stored, which instructions, when read by a group of two or more computer processors in mutual communication, cause one of the computer processors to serve as a master processor, and cause one or more of the computer processors to serve as slave processors,

wherein the instructions cause the master processor to receive an Ordered Binary Decision Diagram (OBDD) representing the model according to an initial order of the variables, the OBDD comprising a number of nodes arranged in rows corresponding respectively to the plurality of the variables, and to assign to each of the one or more slave processors a respective variable among the plurality of the variables, and

wherein the instructions cause each slave processor to reorder the rows of the OBDD by varying a position in the OBDD of one of the rows, which corresponds to the respective variable that is assigned to the slave processor, until at least one of the slave processors identifies a new order for the OBDD, and

wherein the instructions further cause at least one of the computer processors to verify a characteristic of the model against a specification using the new order of the OBDD, and

wherein the instructions cause each of the slave processors to find the new order such that the number of the nodes in the OBDD is reduced relative to the initial order, and

wherein the instructions cause at least two of the computer processors to serve respectively as first and second slave processors, and wherein the instructions cause the master processor to receive first and second new orders, respectively, from the first and

second slave processors and to select the new order from among the first and second new orders so as to minimize the number of the nodes in the OBDD.

29. (Currently amended) The product according to claim [[26]] 28, wherein the instructions cause at least two of the computer processors to serve as slave processors, and further cause the at least two of the processors to reorder the rows by operating simultaneously on a common set of the rows.

30. (Original) The product according to claim 29, wherein the instructions cause the at least two of the processors to operate simultaneously on substantially all the rows of the OBDD.

31.-33. (Cancelled)

34. (Currently amended) The product according to claim [[32,]] 28, wherein the instructions cause the master processor to replace the initial order with the new order, and to repeat assigning a new respective variable to each of the slave processors, so as to cause the slave processors to repeat reordering the rows based on the new order until a predefined reordering criterion is satisfied, and

wherein the instructions cause at least two of the computer processors to serve respectively as first and second slave processors, and wherein the instructions cause the master processor to receive the new order from the first processor, and to communicate the new order to the second processor for use in repeating the reordering of the rows.

35. (Original) The product according to claim 34, wherein the instructions cause the master processor to receive first and second new orders, respectively, from the first and second slave processors, and to select the first new order according to a predefined selection criterion.

36. (Currently amended) The product according to claim [[32]] 28, wherein the instructions cause the at least one of the computer processors to verify the characteristic

of the model by operating on the OBDD while saving data regarding the OBDD in a memory until a predetermined amount of space in the memory has been consumed, and

wherein the instructions further cause the master processor to assign the new respective variable to each of the slave processors and to cause the slave processors to repeat the reordering of the rows so as to reduce the amount of space occupied by the OBDD in the memory due to operating on the OBDD to verify the characteristic.

37.-39. (Cancelled)

40. (Currently amended) ~~The method according to claim 39,~~ A method for modeling a target system, the method comprising:

identifying a plurality of variables that characterize the target system and a Boolean function that is applicable to the variables;

responsively to the Boolean function, arranging the variables in an Ordered Binary Decision Diagram (OBDD) according to an initial order of the variables, the OBDD comprising a number of nodes arranged in rows corresponding respectively to the plurality of the variables;

assigning to each processor, among a group of two or more computer processors, a respective variable among the plurality of the variables; and

using each processor, reordering the rows of the OBDD by varying a position in the OBDD of one of the rows, which corresponds to the respective variable that is assigned to the processor, until at least one of the processors identifies a new order for the OBDD,

wherein reordering the rows comprises operating simultaneously with at least two of the processors on a common set of the rows.

41. (Original) The method according to claim 40, wherein operating simultaneously comprises operating on substantially all the rows of the OBDD using all of the at least two of the processors.

42. (Cancelled)

43. (Currently amended) The method according to claim [[42]] 40, and comprising replacing the initial order with the new order, and repeating the steps of assigning the respective variable and reordering the rows based on the new order until a predefined reordering criterion is satisfied,

wherein the two or more computer processors comprise first and second processors, and wherein reordering the rows comprises receiving the new order from the first processor, and wherein replacing the initial order comprises communicating the new order to the second processor for use in repeating the step of reordering the rows.

44.-50. (Cancelled)

51. (Currently amended) ~~The product according to claim 50,~~ A computer software product for modeling a target system, the product comprising a computer-readable medium in which program instructions are stored, which instructions, when read by a group of two or more computer processors in mutual communication, cause one of the computer processors to serve as a master processor, and cause one or more of the computer processors to serve as slave processors,

wherein the instructions cause the master processor to receive a model of the target system characterized by a plurality of variables and a Boolean function, wherein the model is represented by an Ordered Binary Decision Diagram (OBDD) according to an initial order of the variables, the OBDD comprising a number of nodes arranged in rows corresponding respectively to the plurality of the variables, and

wherein the instructions further cause the master processor to assign to each of the one or more slave processors a respective variable among the plurality of the variables, and

wherein the instructions cause each slave processor to reorder the rows of the OBDD by varying a position in the OBDD of one of the rows, which corresponds to the respective variable that is assigned to the slave processor, until at least one of the slave processors identifies a new order for the OBDD, and

wherein the instructions further cause at least one of the computer processors to verify a characteristic of the model against a specification using the new order of the OBDD, and

wherein the instructions cause at least two of the computer processors to serve as slave processors, and further cause the at least two of the processors to reorder the rows by operating simultaneously on a common set of the rows.

52. (Original) The product according to claim 51, wherein the instructions cause the at least two of the processors to operate simultaneously on substantially all the rows of the OBDD.

53. (Cancelled)

54. (Currently amended) The product according to claim [[53,]] 51, wherein the instructions cause the master processor to replace the initial order with the new order, and to repeat assigning a new respective variable to each of the slave processors, so as to cause the slave processors to repeat reordering the rows based on the new order until a predefined reordering criterion is satisfied, and

wherein the instructions cause at least two of the computer processors to serve respectively as first and second slave processors, and wherein the instructions cause the master processor to receive the new order from the first processor, and to communicate the new order to the second processor for use in repeating the reordering of the rows.